

ABSTRACT

Under the control of a processor executing a program, the timing margin of an electronic system can be improved by a series of operations that set the relative phase of receive and distributed clock signals from a number of given values, a relative phase of transmit and distributed clock signals from a number of given values, instruct an integrated circuit (IC) die to drive a sequence of outgoing data symbols and receive a sequence of incoming data symbols at those relative phase settings, and compares the outgoing symbols to the incoming symbols. A result of the comparison is recorded. The operations are repeated for other combinations of the discrete transmit and receive phase values. The relative phases are then set to a pair of values taken from the discrete transmit and receive phase values, which are closest to yielding a balanced timing margin as determined from the results of the comparisons.

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